UTTAM SINGISETTI
uttamsin@buffalo.edu
www.eng.buffalo.edu/~uttamsin/

Assistant Professor
Electrical Engineering
University at Buffalo, Buffalo, NY 14260, USA
Tel: (716)645-1536 Fax: (716) 645 3656

Research Interests

Advanced GaN and novel III-N devices for THz electronics, Nano-electronics in emerging materials, Energy efficient nano-electronics, Transport in III-N hetero-structures

Education

PhD, University of California, Santa Barbara (UCSB),
Electrical and Computer Engineering. [Sep 2009].
Dissertation : "$In_{0.53}Ga_{0.47}As$ MOSFETs with 5 nm channel and self-aligned Source/Drain by MBE regrowth."
Advisor : **Dr Mark Rodwell,** Professor, Electrical Engineering, University of California at Santa Barbara.

MS, Arizona State University,
Interdisciplinary Science and Engineering of Materials Program, [May 2004].
Thesis: "Ultra-shallow junctions for sub-100nm Si n-MOSFETs"
Advisor : **Dr Stephen M Goodnick,** Professor, Electrical Engineering, Arizona State University

Bachelor of Technology, **Indian Institute of Technology (IIT), Madras,**
Department of Materials Science and Engineering, India [May 2001]. Concentration in Electronic Materials.

Experience

Assistant Professor,
Electrical Engineering, University at Buffalo, Sep 2011-present.
Teaching: RF/Microwave Circuits I (EE409/EE569), Spring 2012, Fall 2012, Senior/ Graduate course
Analog Integrated Circuit Layout (EE449/EE594), Fall 2011, Spring 2013, Senior/ Graduate course

Assistant Project Scientist,
Prof. Umesh Mishra Research Group, **Electrical and Computer Engineering, UCSB**, Sep 2009-Aug 2011.

Developed ultra-scaled N-polar GaN enhancement mode devices for mm-wave and sub-mm wave operation.
Demonstrated record high f_t, and record low on-resistance for enhancement mode GaN devices in the novel N-polar GaN technology as compared to the mature Ga-polar enhancement mode devices.
Optimized channel design for improved mobility and low output conductance.

Graduate Student Researcher,
Electrical and Computer Engineering, UCSB- Sep 2004-Sep 2009

Demonstrated fully self-aligned InGaAs MOSFETs with ultra-scaled (5 nm) channel for beyond-22 nm VLSI logic application. A multi-university collaborative effort with Prof. Paul McIntyre (Stanford University), Prof. Art Gossard (UCSB), Prof. Yuan Taur (UCSD).
Designed and first demonstrated a scalable MOSFET process with novel self-aligned n^{++} InAs Source/Drain by MBE regrowth and self-aligned *in-situ* Mo S/D contacts to eliminate source starvation.
Performance, electron transport and high-k interface properties evaluation by DC I-V, and C-V measurements.

Developed ultra-low contact resistance to $In_{0.53}Ga_{0.47}As$ with applications in III-V MOSFETs and InP DHBTs.

Ion implanted sub-collector InP Double Hetero-structure Bipolar Transistors (DHBT) for sub-mm-wave mixed signal applications.

Summer Research Intern,
Advanced Transistor and Nanotechnology group, Intel Corporation, Jun-2006-Sep-2006

RF measurement and characterization of Silicon Tri-gate NMOS and PMOS devices. Developed a simplified small signal equivalent circuit model to accurately model Tri-gate RF performance and extract parasitic capacitances and resistance. (Mentor: **Dr Suman Datta**, Intel, Oregon, Now at Pennsylvania State University)

Graduate Research Assistant,
Center for Solid State Electronics Research, Electrical Engineering, Arizona State University- May-2002 –May-2004

Si ultra-shallow n^{++} junctions by rapid thermal diffusion of spin-on dopants and two-dimensional electrical characterizations.
Integration of sub 100nm Si-NMOSFETs and Si Single Electron Transistors (SET) on SOI wafers.

Undergraduate Researcher,
Magnetism and Magnetic Materials Lab, Dept of Physics, IIT Madras India, May 2000-May 2001
Study of amorphous magnetic materials with applications in sensors, power transformers and magnetic recordings.

Honors and Awards

Best Poster award at the 2010 International Workshop on Nitride Semiconductors (IWN 2010).
Co-author of Best Student Paper in Indium Phosphide and Related Materials Conference 2010 (IPRM 2010).
Best Student Paper finalist in Indium Phosphide and Related Materials Conference 2009 (IPRM 2009).
Merit Award for Highest Junior GPA in the class at Indian Institute of Technology (IIT) Madras.

Professional Services / Activities

Technical Program Committee member: 2014 International Workshop on ZnO and Related Semiconductors, and 2013 International Semiconductor Device Research Symposium (ISDRS 2013).
Organizer of Workshop on Oxide Semiconductors: Properties and Applications, at the University at Buffalo to be held on June 4th, 2012.
Reviewer IEEE Electron Device Letters, IEEE Transactions on Electron Devices, Physica Status Solidi (c), and Electro chemical and solid state letters.
Member of IEEE, IEEE Electron Devices Society, IEEE Microwave Theory and Techniques Society, American Physics Society.

Research Publications

Journal Publications:

1. "High-performance N-polar GaN enhancement-mode device technology", U. Singisetti, M. H. Wong, U. K. Mishra", Semiconductor Science and Technology, vol. 28, no. 7, p. 074006, 2013.
2. "N-polar GaN epitaxy and high electron mobility transistors", M. H. Wong, S. Keller, Nidhi, S. Dasgupta, D. Denninghoff, S. Kolluri, D. F. Brown, J. Lu, N. A. Fichtenbaum, E. Ahmadi, U. Singisetti, A. Chini, S. Rajan, S. P. DenBaars, J. S. Speck, and U. K. Mishra", Semiconductor Science and Technology, vol. 28, no. 7, p. 074009, 2013.
3. "Anomalous output conductance in N-polar GaN based High-Electron Mobility Transistors", M. H. Wong, U. Singisetti, J. Lu, J. S. Speck, U. K. Mishra, *IEEE Transactions on Electron Devices,* vol 59, no. 11, 2988-2995, 2012.
4. "Interface roughness scattering in ultra-thin N-polar GaN quantum well channels", U.Singisetti, M. H. Wong, and U. K. Mishra, *Applied Physics Letters.*, vol 101, no.1, pp. 012101-4, 2012.
5. "Enhancement-mode N-polar GaN MOS-HFET with 5-nm GaN channel, 510 mS/mm gm and 0.66 Ohm-mm Ron", U.Singisetti, M. H. Wong, J. S. Speck, and U. K. Mishra, IEEE Electron Device Letters, vol. 33, no.1, pp. 26-28, 2012.

6. "Enhancement-mode N-polar GaN MISFETs with current gain cutoff frequency (f_t) of 120 GHz", U.Singisetti, M. H. Wong, S. Dasgupta, J. S. Speck, and U. K. Mishra, *Applied Physics Express,* vol. 4, no. 2, p. 024103, 2011.
7. "Enhancement-mode N-polar GaN MISFETs with self-aligned source/drain regrowth", U. Singisetti, M. H. Wong, S. Dasgupta, Nidhi, B. L. Swenson, B. J. Thibeault, J. S. Speck and U. K. Mishra, *IEEE Electron Device Letters*. Vol. 32, no. 2, pp. 137-139, 2011.
8. "Self-aligned technology for N-polar GaN/Al(Ga)N MIS-HEMTs", Nidhi, S. Dasgupta, D. Brown, U. Singisetti, S. Keller, J. S. Speck and U. K. Mishra; *IEEE Electron Device Letters*., vol. 32, no.1, pp. 33-35, 2011.
9. "Ex-situ Ohmic contacts to n-InGaAs", A. Baraskar, M. A. Wistey, V. Jain, E. Lobisser, U. Singisetti, G. Burek, Y. J. Lee, B. J. Thibeault, A. C. Gossard, M. J. W. Rodwell, *J. Vac. Sci. Tech. B*, 28, C517, 2010.
10. "$In_{0.53}Ga_{0.47}As$ channel MOSFETs with self-aligned InAs Source/Drain formed by MEE regrowth", U.Singisetti, M.A. Wistey, G.J. Burek, A.K. Baraskar, J. Cagnon, B.J. Thibeault, A.Gossard, S. Stemmer, M. Rodwell, E.Kim, B.Shin, P.C McIntyre; *IEEE Electron Device Letters*, Vol. 30, No. 11, pp 1128-1130,2009.
11. "III-V/Ge Channel Engineering for Future CMOS", M. Wistey, U. Singisetti, G. Burek, E. Kim, B. J. Thibeault, A. Nelson, J. Cagnon, Y. -J. Lee, S. R. Bank, S. Stemmer, P. C. McIntyre, A. C. Gossard, and M. J. Rodwell, *ECS Trans*. 19 (5), 361, 2009.
12. " InGaAs channel MOSFET with novel self-aligned source/drain MBE regrowth technology", U. Singisetti, M.A. Wistey, G.J. Burek, E. Arkun, Y.Sun, E.J. Kiwera, B. J. Thibeault, A.C. Gossard, C.Palmstrom, and M.J.W. Rodwell; *physica solidi status (c);* Vol. 6, No. 6, pp. 1394-1398, 2009.
13. "Ultralow resistance, nonalloyed Ohmic contacts to n-InGaAs", A. Baraskar, M. A. Wistey, V. Jain, U. Singisetti, G. Burek, B. J. Thibeault, Y. J. Lee, A. C. Gossard and M. J. W. Rodwell,, *J. Vac. Sci. Tech. B,* 27, 2036, 2009.
14. "Height-selective etching for regrowth of self-aligned contacts using MBE", G.J. Burek, M.Wistey, U.Singisetti, A.Nelson, B.Thibeault, S.Bank,A.Gossard, M.Rodwell; *Journal of Crystal Growth;* Vol 311, pp 1984-1987.
15. "ErAs epitaxial Ohmic contacts to InGaAs/InP"; U.Singisetti, J. Zimmerman, M.A.Wistey, J.Cagnon, B.Thibeault, A. Gossard, S.Stemmer, M.Rodwell, S.R.Bank; *Applied Physics Letters*; Vol 94, pp 083505.
16. "Ultra-Low resistance *in-situ* Ohmic contacts to InGaAs/InP", U.Singisetti, M.A.Wistey, J.Zimmerman, B.Thibeault, A.Gossard, M.Rodwell; *Applied Physics Letters;* Vol 93, pp183502.
17. "Collector-Pedestal InGaAs/InP DHBTs Fabricated in a Single-Growth, Triple-Implant Process", N. Parthasarathy, C. Kadow, Z. Griffith, U. Singisetti, M. J. Rodwell; *IEEE Electron Device Letters,* Vol 27 (5), pp 313-316.
18. "Two-dimensional electrical Characterization of ultrashallow Source/Drain Extensions for nanoscale MOSFETs", U. Singisetti, M.R.McCartney, J.Li, P.S.Chakraborty, S.M.Goodnick, T.J.Thornton, M.N.Kozicki; *Superlattices and Microstructures,* Vol 34, pp 301-310, 2004.
19. "Electron Holographic Characterization of Nanoscale Charge Distribution for Ultra Shallow PN Junctions in Si", P.S. Chakraborty, M.R. McCartney, J. Li, C. Gopalan, U. Singisetti, S.M. Goodnick, T.J. Thornton, M.N. Kozicki; Physica E: Low-dimensional Systems and Nanostructures, Vol 19/1-2, pp 167-172, 2003.

Conference Publications:

1. "A 50 nm gate length InN tri-gate FET design with gm of 1.07 mS/μm and f_t of 495 GHz ", K. Ghosh, and U. Singisetti, *2013 IEEE Device Research Conference*, University of Notre Dame, USA.
2. "Vertically scaled 5 nm GaN channel Enhancement-mode N-polar GaN MOS-HFET with 560 mS/mm g_m and 0.76 Ω-mm R_{on} ", U. Singisetti, M. H. Wong, J. S. Speck, U. K. Mishra, *Late News, 2011 Device Research Conference***,** Santa Barbara.
3. "Anomalous output conductance in N-polar GaN based MIS-HEMTs", M. H. Wong, U. Singisetti, J. Lu, J. S. Speck, U. K. Mishra, *2011 Device Research Conference*, Santa Barbara.
4. "Interface roughness scattering in ultra-thin GaN channels in N-polar enhancement-mode GaN MISFETs", U. Singisetti, M. H. Wong, J. S. Speck and U. K. Mishra, *2011 International Symposium on Compound Semiconductors*, Berlin, 2011.
5. "100 nm gate length self-aligned E-mode N-polar GaN MISFETs with current gain cutoff frequency (f_t) of 120 GHz", U. Singisetti, M. H. Wong, S. Dasgupta, Nidhi, B. L. Swenson, B. J. Thibeault, J. S. Speck and U. K. Mishra, *2010 International Workshop on Nitride Semiconductors*, Tampa, 2010.

6. "Scalable E-mode N-polar GaN MISFET devices and process with self-aligned source/drain regrowth", U Singisetti, M. H. Wong, S. Dasgupta, Nidhi, B. L. Swenson, B. J. Thibeault, J. S. Speck and U. K. Mishra, *2010 Device Research Conference*, University of Notre Dame, South Bend, IN, USA.
7. **[Plenary]** "III-V MOSFETs: Scaling Laws, Scaling Limits, Fabrication Processes", M. J. W. Rodwell, U. Singisetti, M.Wistey, G. J. Burek, A. Carter, A. Baraskar, J. Law, B. J. Thibeault, Eun Ji Kim, B. Shin, Yong-ju Lee, S. Steiger, S. Lee, H. Ryu, Y. Tan, G. Hegde, L. Wang, E. Chagarov, A.C. Gossard, W. Frensley, A. Kummel, C. Palmstrøm, Paul C McIntyre, T. Boykin, G. Klimek, P. Asbeck, *IEEE 22nd International Conference on Indium Phosphide and Related Materials* May 31-June 4, 2010, Kagawa, Japan.
8. "A Self-Aligned Epitaxial Regrowth Process for Sub-100-nm III-V FETs", M. J.W. Rodwell, A. D. Carter, G. J. Burek, M. A. Wistey, B. J. Thibeault, A. Baraskar, U. Singisetti, Byungha Shin, E. Kim, J. Cagnon, Y.-J. Lee, S. Stemmer, P. C. McIntyre, A. C. Gossard, C. Palmstrøm, D. Wang, B. Yue, P. Asbeck, Y. Taur, *2010 MRS Spring Meeting- April 5-9, 2010, San Francisco.*
9. "THz Transistors: Design and Process Technologies", M. J.W. Rodwell, V. Jain, E. Lobisser, A. Baraskar, M. A. Wistey, U. Singisetti, G. J. Burek, B. J. Thibeault, A. C. Gossard, E. J Kim, P. C. McIntyre, B. Yu, P. Asbeck, Y. Taur, *2010 Government Microcircuit Applications and Critical Technology Conference,* March 22-25, 2010, Reno, NV.
10. "In0.53Ga0.47As MOSFETs with 5 nm channel and self-aligned InAs source/drain by MBE regrowth", U.Singisetti, M.A. Wistey, G.J. Burek, A.K. Baraskar, J. Cagnon, B.J. Thibeault, A.Gossard, S. Stemmer, M. Rodwell, E.Kim, B.Shin, P.C McIntyre, *WOCSEMMAD 2010*.
11. "Ex-situ Ohmic Contacts to n-InGaAs Prepared by Atomic Hydrogen Cleaning", A. Baraskar, M.A. Wistey, E. Lobisser, V. Jain, U. Singisetti, G. Burek, Y.J. Lee, B. Thibeault, A. Gossard, M. Rodwell, *37th Conference on the Physics and Chemistry of Surfaces and Interfaces*, Jan. 10-14, 2010, Santa Fe, New Mexico, USA.
12. "Sub-100-nm Process Technologies For THz InP HBTs & MOSFETs", M. J.W. Rodwell, E. Lobisser, V. Jain, A. Baraskar, M. A. Wistey, U. Singisetti, G. J. Burek, B. J. Thibeault, A. C. Gossard, E. Kim, P. C. McIntyre, B. Yu, P. Asbeck, Y. Taur, *2009 International Workshop on Terahertz Technology*, Osaka, Japan, Nov. 30 -Dec. 3, 2009.
13. "Process Technologies for Sub-100-nm InP HBTs and InGaAs MOSFETs", M. J. W. Rodwell, M. A. Wistey, U. Singisetti, G. J. Burek, E. Kim, A. Baraskar, J. Cagnon, Y.-J. Lee, S. Stemmer, P. C. McIntyre, A.C. Gossard, B. Yu, P. Asbeck, Y. Taur, *8th Topical Workshop on Heterostructure Microelectronics*, Nagano, Japan, Aug. 2009.
14. "Improved Regrowth of Self-Aligned Ohmic Contacts for III-V FETs", M.A. Wistey, A.K. Baraskar, U. Singisetti, B. Shin, E. Kim, G.J. Burek, P.C. Mcintyre, M.J.W. Rodwell, and A.C. Gossard, *26th North American Molecular Beam Epitaxy Conference (NAMBE 2009)*, Princeton, New Jersey, August 2009.
15. "Enhancement Mode In(0.53)Ga(.47)As MOSFET with Self-Aligned Epitaxial Source/Drain", U.Singisetti, M.A. Wistey, G.J. Burek, A.K. Baraskar, J. Cagnon, B.J. Thibeault, A.Gossard, S. Stemmer, M. Rodwell, E.Kim, B.Shin, P.C McIntyre; *2009 TECHCON*, Renaissance Hotel, Austin, TX, September 14 – 15, 2009.
16. "0.37 mS/μm InGaAs MOSFET with 5 nm Channel and self-aligned Source/Drain regrowth", U.Singisetti, M.A. Wistey, G.J. Burek, A.K. Baraskar, J. Cagnon, B.J. Thibeault, A.Gossard, S. Stemmer, M. Rodwell, E.Kim, B.Shin, P.C McIntyre; *2009 Device Research Conference*, Pennsylvania State University, College Park, PA.
17. "Improved Migration Enhanced Epitaxy for Self-aligned InGaAs Devices", M.Wistey, U.Singisetti, A. Baraskar, G.Burek, M.Rodwell, A.Gossarsd; *2009 Electronic Materials Conference,* Pennsylvania State University, PA.
18. "High Doping Effects on the In-Situ and Ex-Situ Ohmic Contacts to n-InGaAs", A. K. Baraskar, M. A. Wistey, V. Jain, U. Singisetti, G. Burek, B. J. Thibeault, Y. J. Lee, A. C. Gossard, and M. J. W. Rodwell, *2009 Electronic Materials Conference,* Pennsylvania State University, PA,USA
19. "Ultra-low contact resistance for Self-aligned HEMT structures on N-polar GaN by MBE regrowth of InGaN-based contact layers", Nidhi, S.Dasgupta, M.Hong, U.Singisetti, M.Wistey, M.Rodwell, U.Mishra; *2009 Electronic Materials Conference,* Pennsylvania State University, PA,USA.
20. "Enhancement Mode InGaAs MOSFET with self-aligned Epitaxial Source/Drain regrowth", U.Singisetti, M.A. Wistey, G.J. Burek, A.K. Baraskar, J. Cagnon, B.J. Thibeault, A.Gossard, S. Stemmer, M. Rodwell, E.Kim, B.Shin, P.C McIntyre; *Indium Phosphide and Related Materials Conference 2009*, Newport Beach, CA, USA.
21. "Effect of Surface Preparations on Contact Resistivity of TiW to Highly Doped n-InGaAs", V. Jain, A.K. Baraskar, M.A. Wistey, U. Singisetti, Z. Griffith, E. Lobisser, B. J. Thibeault, A.C. Gossard, M. J. W. Rodwell, *Indium Phosphide and Related Materials Conference 2009*, Newport Beach, CA, USA.
22. "III-V/Ge Channel Engineering for Future CMOS", M.A.Wistey, U.Singisetti, G.J. Burek, E.Kim, B.J. Thibeault, A.Nelson, J.Cagnon, Y.J.Lee, S.R. Bank, S.Stemmer, P.C. McIntyre, A.C. Gossard, M. Rodwell, presented at *215th ECS Meeting 2009,* San Francisco, May, 2009.

23. "Ultra-low resistance, non-alloyed ohmic contacts to n-InGaAs", A. K. Baraskar, M. A. Wistey, V. Jain, U.Singisetti, G. Burek, B. J.Thibeault, Y. J. Lee, A. C. Gossard and M. J. W. Rodwell, *Physics and Chemistry of Semiconductor Interfaces,* January 2009, Santa Barbara.
24. " InGaAs channel MOSFET with novel self-aligned source/drain MBE regrowth technology ", U. Singisetti, M.A. Wistey, G.J. Burek, E. Arkun, Y.Sun, E.J. Kiwera, B. J. Thibeault, A.C. Gossard, C.Palmstrom, and M.J.W. Rodwell, *International Symposium on Compound Semiconductors*, Europa-Park, Freiburg, Germany, September 21 - 24, 2008.
25. "Regrowth of Self-Aligned, Ultra Low Resistance Ohmic Contacts on InGaAs", M.A. Wistey, G.J. Burek, U. Singisetti, A. Nelson, B.J. Thibeault, S.R. Bank, M.J.W. Rodwell, and A.C. Gossard, *5th International Conference on Molecular Beam Epitaxy* August 3 – 8, 2008, University of British Columbia, Vancouver, Canada.
26. "MBE Regrown Contacts for InGaAs Field Effect Transistors", M.Wistey, U.Singisetti, G.Burek, J.Cagnon, S.Stemmer, M.Rodwell, A.Gossard, presented at *2008 Electronic Materials Conference.* June 2008, Santa Barbara,CA.
27. **[Invited]** "Technology Development & Design for 22 nm InGaAs/InP-channel MOSFETs", M. J. W. Rodwell, U. Singisetti, M. Wistey, G. Burek, A. Gossard, C. Palmstrøm, E. Arkun, P. Simmonds, S. Stemmer, R. Engel-Herbert, Y. Hwang, Y. Zheng, P. Asbeck, Y. Taur, M. V. Fischetti, B. Yu, D. Wang, Y. Yuan, C. Sachs, A. Kummel, P. McIntyre, C. Van de Walle, and J. Harris, *Indium Phosphide and Related Materials Conference 2008*.
28. "On the Feasibility of low-THz InP HBTs", M. Rodwell, Z. Griffith, E. Lind, U. Singisetti, M. Wistey, A. Gossard, *2008 Government Microcircuit Applications and Circuit Technology Conference*, Mar 17-20, 2008, Las Vegas, NV.
29. "Ultra-Low Resistance Ohmic contacts to InGaAs/InP", U. Singisetti, A. M. Crook, J.D. Zimmerman, M. A. Wistey, A.C. Gossard, and M. J. Rodwell; *2007 Device Research Conference*, University of Notre Dame, South Bend, IN, USA, Jun 2007.
30. "On the Feasibility of few-THz Bipolar Transistors", M Rodwell, E. Lind, Z. Griffith, A.M. Crook, S.R. Bank, U. Singisetti, M. Wistey, G. Burek, A.C. Gossard, *2007 IEEE Bipolar/BiCMOS Circuits and Technology Meeting, 2007*. Sept. 30 2007-Oct. 2 2007 Page(s):17 - 21, Boston, Mass.
31. "Frequency Limits of InP-based Integrated Circuits", Mark Rodwell, E. Lind, Z. Griffith, S. R. Bank, A. M. Crook, U. Singisetti, M. Wistey, G. Burek, A.C. Gossard, *IEEE Int. Conf. Indium Phosphide and Related Materials*, Matsue, Japan, May 14-18, 2007.
32. "MBE growth of ErAs/In(Ga)As epitaxial ultra-low resistance ohmic contacts", S.R. Bank, U. Singisetti, A. M. Crook, J.D. Zimmerman, J. M. O. Zide, A.C. Gossard, and M. J. Rodwell; presented at the *2006 North American MBE Conference*, Durham, NC, USA, Oct 2006.
33. "Two-dimensional electrical Characterization of ultrashallow Source/Drain Extensions for nanoscale MOSFETs", U Singisetti, M. R. McCartney, J. Li, P. S. Chakraborty, S. M.Goodnick, T. J. Thornton, M. N. Kozicki; *Sixth International Conference on New Phenomena in Mesoscopic Systems and Fourth International Conference on Surfaces and Interfaces of Mesoscopic Devices*, Maui, Hawaii, USA, December 2003.
34. "Developing Bipolar Transistors for Sub-mm-Wave Amplifiers and Next-Generation (300 GHz) Digital Circuits", Mark Rodwell, Z. Griffith, N. Parthasarathy, E. Lind, C. Sheldon, S. R. Bank, U. Singisetti, M. Urteaga, K. Shinohara, R. Pierson, P. Rowell, *Device Research Conference, June 2006*, State College PA.
35. "Frequency Limits of Bipolar Integrated Circuits", M.Rodwell, Z.Griffith, N.Parthasarathy, U.Singisetti, V.Paidi, M.Urteaga, R.Pierson, B.Brar; *IEEE MTT-S International Microwave Symposium Digest, 2006*. pp 329-332.
36. "Selectively implanted subcollector DHBTs and implanted pedestal-subcollector InP DHBTs", N. Parthasarathy, Z. Griffith, C. Kadow, U. Singisetti, M. Urteaga, K. Shinohara, B. Brar and M. J. Rodwell; presented at the *Indium Phosphide and Related Materials Conference*, Princeton University, USA, May 2006.
37. "InP HBT Digital ICs and MMICs in the 140-220 GHz band", Mark Rodwell, Z. Griffith, V. Paidi, N. Parthasarathy, C. Sheldon, U. Singisetti, M. Urteaga , R. Pierson, P. Rowell, B. Brar, 2005 Joint 30th *International Conference on Infrared and Millimeter Waves and 13th International Conference on Terahertz Electronics*, September 19-23, 2005 Williamsburg, Virginia USA.
38. "Electron Holographic Characterization of Nanoscale Charge Distribution for Ultra Shallow PN Junctions in Si", P. S. Chakraborty, M. R. McCartney, J. Li, C. Gopalan, U. Singisetti, S. M. Goodnick, T.J.Thornton, M.N.Kozicki; *The Fourth International Symposium on Nanostructures and Mesoscopic Systems*, Tempe, February 17-21, 2003.